CLAIMS

1. A controllable rectifying element, comprising a bipolar transistor having a current input terminal connected to a control terminal by a first switch and having a current output terminal directly connected to the control terminal by a second switch, the turn-off and turn-on phases of the first and second switches being complementary and depending on the state desired for the rectifying element.

2. The rectifying element of claim 1, further comprising a circuit for controlling the first and second switches according to the state of a signal for enabling/disabling the rectifying element.

3. The rectifying element of claim 1, wherein said switches are formed of P-channel MOS transistors having their respective gates connected to the control terminal of the bipolar transistor via current sources.

4. The rectifying element of claim 2, wherein said switches are formed of P-channel MOS transistors having their respective gates connected to the control terminal of the bipolar transistor via current sources.

5. The rectifying element of claim 4, wherein the control circuit comprises two N-channel MOS transistors connecting the respective gates of the P-channel MOS transistors to ground, said N-channel MOS transistors being respectively controlled by the enable signal and by its inverse.

6. The rectifying element of claim 1, wherein said bipolar transistor is a PNP transistor.

7. The rectifying element of claim 1, wherein said bipolar transistor is an NPN transistor.

8. A voltage converter of D.C./D.C. type comprising the rectifying element of claim 1.

9. A rectifying circuit comprising:

a supply transistor having an input terminal, an output terminal and a control terminal;

a first switch for selectively coupling the input terminal of the supply transistor to the control terminal of the supply transistor;

a second switch for selectively coupling the output terminal of the supply transistor to the control terminal of the supply transistor; and

a control signal line coupled to the first and second switching elements that selectively enables one of the switching elements to connect the respective terminals to the control terminal and disables the other of the switching elements from connecting their respective terminal to the control terminal.

10. The rectifying circuit according to claim 9 wherein the supply transistor is a bipolar transistor.

11. The rectifying circuit according to claim 9 wherein said first and second switches are composed of MOS transistors.

12. The rectifying circuit according to claim 10 further including an inverter positioned between the control signal line and the first and second switches, respectively, ensuring that the two switches are in opposite states at all times.

13. The rectifying circuit according to claim 12, further including:

respective MOS transistors coupled to control gates of the first and second MOS transistors acting as the switches, the inverter being coupled to the gate of one of the additional MOS transistors and not to the gate of the other additional MOS transistors.

14. The rectifying circuit according to claim 9, further including first and second current sources extending from the control terminal of the supply transistor to respective gate terminals of the MOS transistors acting as switches.

15. The rectifying circuit according to claim 9, wherein said input control signal line provides an enable signal for switching the rectifier element on.

16. The rectifying circuit according to claim 9, further including an inductor coupled to the input of the supply transistor and a switching element coupled between the inductor and the input terminal to the supply transistor for selectively coupling the input of the supply transistor to the inductor output or to a voltage reference source.

17. The rectifier circuit according to claim 16, wherein said voltage reference source is ground.

18. The rectifying circuit according to claim 11 wherein the rectifier circuit is integrated onto a single silicon substrate and the area in silicon substrate occupied by the MOS transistors is smaller than the area consumed by the supply transistor and the difference in area occupied is approximately proportional to the expected current flowing through the supply transistor divided by the gain of the supply transistor.